ADDENDUM

STD BUS Multifunction 8088 CPU/Communication Card 7864

7864 USER'S MANUAL

The 7864 8088 CPU/Communication Card is now expanded to include a Single Master version, 7864-3. The Multimaster version remains the 7864-1. To document both versions, both cards will temporarily be shipped with the 7864 User's Manual and this Addendum.

NOTE

The following documents, which are sent with the 7864 User's Manual, are still valid and necessary, and are not incorporated into this Addendum:

Errata Sheet (Document #112339-001)
(New 7864 I/O Address Port Assignments)

Errata Sheet (Document #112498-001)
(Multimaster Arbiter Change)

Addendum (Document #112425-001)
(Multimaster Timing Diagram)

This Addendum is divided into two segments:

PART I Covers new changes to the existing 7864 Multimaster manual. **The changes specified for Sections 1 and 5 apply to both the 7864-1 and 7864-3 cards.** Section 1 now includes the latest 8088 STD BUS Timing Specification. Section 5 contains the current Schematic and Assembly Documentation.

PART II Applies only to the 7864-3 Single Master card.

PART I

SECTION 1. SPECIFICATIONS

NOTE

This information applies to **both** the 7864-1 and the 7864-3.

Page 1-1, under "Features"

DELETE: The asterisk after "• Up to 64K bytes of onboard RAM (32K by 8 devices*)"

DELETE: The footnote "~~*Not available at publication~~"

NOTE: 32K by 8 static RAMs are now available.

Page 1-6, under "TIMING SPECIFICATIONS"

ADD: "The critical timing parameters as defined by the proposed IEEE P961/D4 STD BUS Standard (February 4, 1985 document, Figures 9 and 10) are listed below. The 7864 meets the September 15, 1985 STDMG STD-8088 revision 2.0 Specification.

Critical Timing

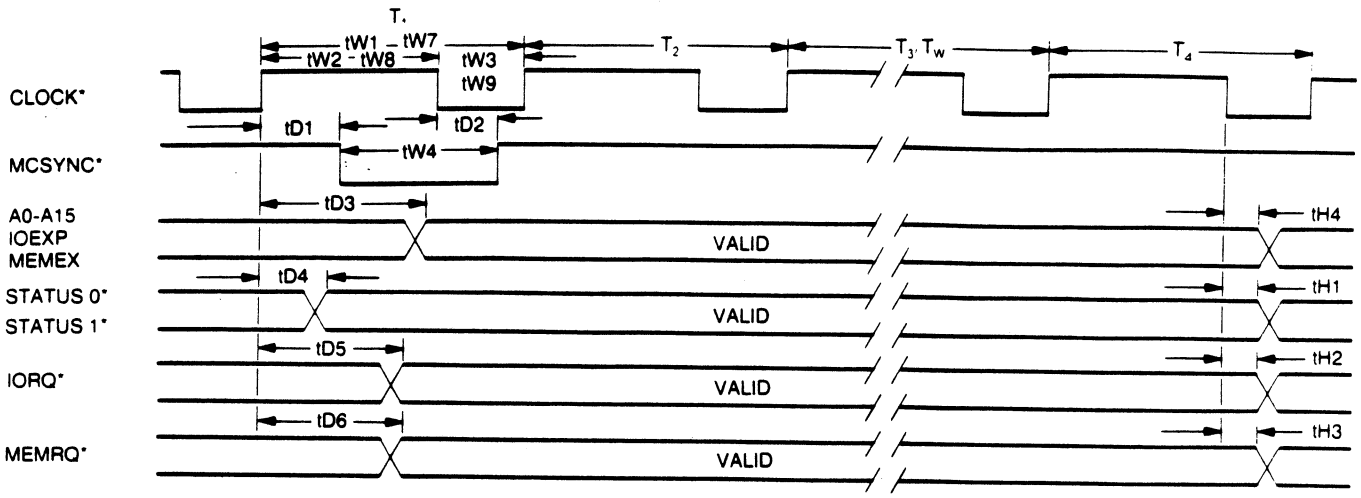
- tAR, maximum available Read Access Time, equals 210 nanoseconds.

- tSWD, minimum available Write Data Setup Time, equals 333 nanoseconds.

- tHWD, minimum available Write Data Hold Time, equals 60 nanoseconds."

Pages 1-7 through 1-11, Timing Diagrams

REPLACE: All timing diagrams with those on the following pages.

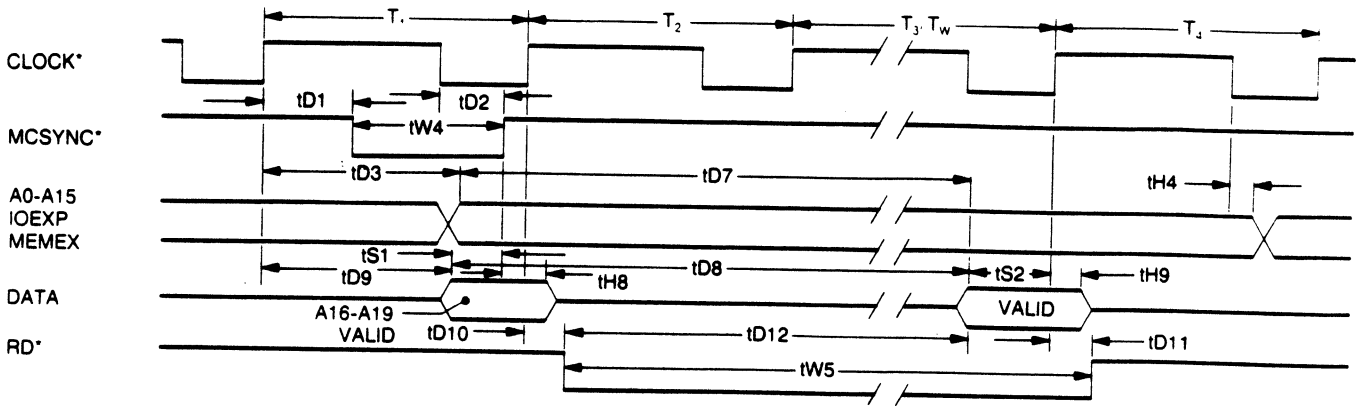


SYMBOL	PARAMETER	4.9152 MHz MIN	4.9152 MHz MAX
tW1	8088 CLOCK* period	201	205
tW2	8088 CLOCK* high width	133	137
tW3	8088 CLOCK* low width	66	70

SYMBOL	PARAMETER	4.9152 MHz MIN	4.9152 MHz MAX
tD1	Delay from CLOCK* to MCSYNC* low	121	
tD2	Delay from CLOCK* to MCSYNC* high		102
tD3	Delay from CLOCK* to Address 0-15, MEMEX,IOEXP		125
tD4	Delay from CLOCK* to STATUS*		57
tD5	Delay from CLOCK* to IORQ*		57
tD6	Delay from CLOCK* to MEMRQ*		57
tH1	STATUS* hold after CLOCK*	12	
tH2	IORQ* hold after CLOCK*	12	
tH3	MEMRQ* hold after CLOCK*	4	
tH4	Address 0-15, MEMEX, IOEXP hold after CLOCK*	5	
tW4	MCSYNC* pulse width	68	

All times given in nanoseconds

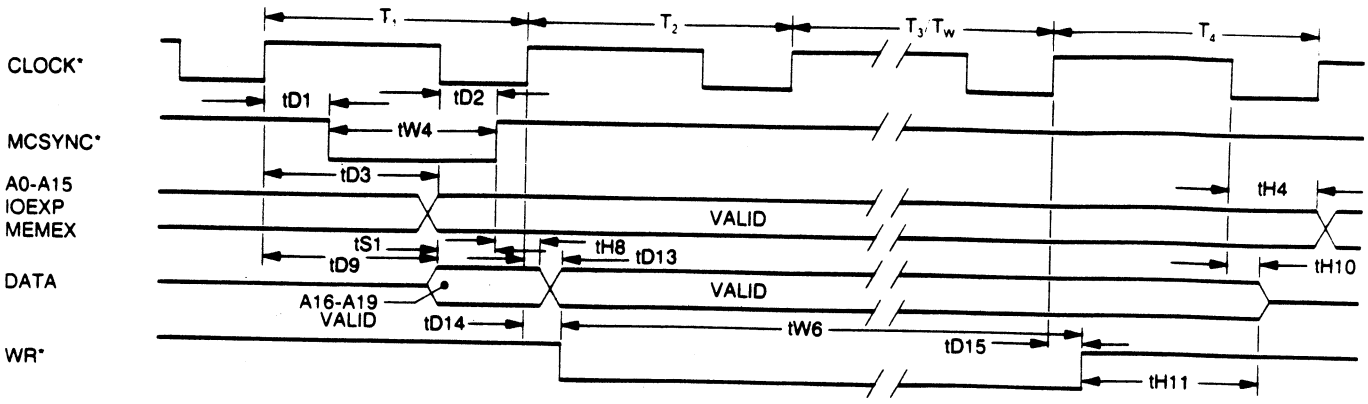
Figure 1-8. Bus Status Timing



SYMBOL	PARAMETER	4.9152 MHz MIN	4.9152 MHz MAX
tD1	Delay from CLOCK* to MCSYNC* low	121	
tD2	Delay from CLOCK* to MCSYNC* high		102
tD3	Delay from CLOCK* to Address 0-15, MEMEX,IOEXP		125
tD7	Delay from Address 0-15, MEMEX, IOEXP to data valid	433	
tD8	Delay from Address 16-19 to data valid	433	
tD9	Delay from CLOCK* to Address 16-19		125
tD10	Delay from CLOCK* to RD* low	116	155
tD11	Delay from CLOCK* to RD* high	48	87
tD12	Delay from RD* to Data valid	210	
tH4	Address 0-15, MEMEX, IOEXP hold after CLOCK*	5	
tH8	Address 16-19 hold after MCSYNC*	53	
tH9	RD* data hold after CLOCK*	6	
tS1	Address 16-19 setup to MCSYNC*	64	
tS2	Data setup to CLOCK*	52	
tW4	MCSYNC* pulse width	68	
tW5	RD* pulse width	339	

All times given in nanoseconds

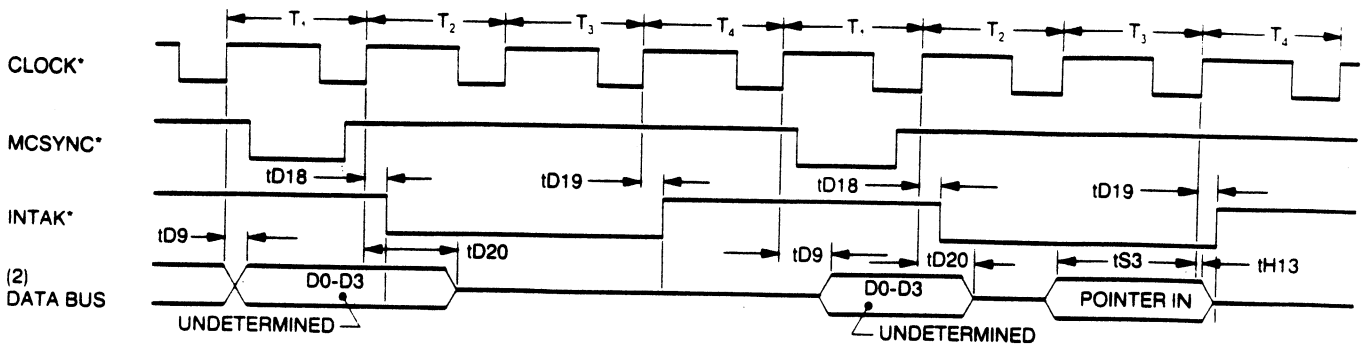
Figure 1-9. Bus Read Timing



SYMBOL	PARAMETER	4.9152 MHz MIN	4.9152 MHz MAX
tD1	Delay from CLOCK* to MCSYNC* low	121	
tD2	Delay from CLOCK* to MCSYNC* high		102
tD3	Delay from CLOCK* to Address 0-15, MEMEX, IOEXP		125
tD9	Delay from CLOCK* to Address 16-19		125
tD13	Delay from CLOCK* to Data Valid		119
tD14	Delay from CLOCK* to Advanced WR* low	48	87
tD15	Delay from CLOCK* to Advanced WR* high	48	87
tH4	Address 9-15, MEMEX, IOEXP hold after CLOCK*	5	
tH8	Address 16-19 hold after MCSYNC*	53	
tH10	WR* data hold after CLOCK*	10	
tH11	Data hold after Advanced WR* high	58	
tS1	Address 16-19 setup to MCSYNC*	64	
tW4	MCSYNC* pulse width	68	
tW6	Advanced WR* pulse width	407	

All times given in nanoseconds

Figure 1-10. Bus Write Timing

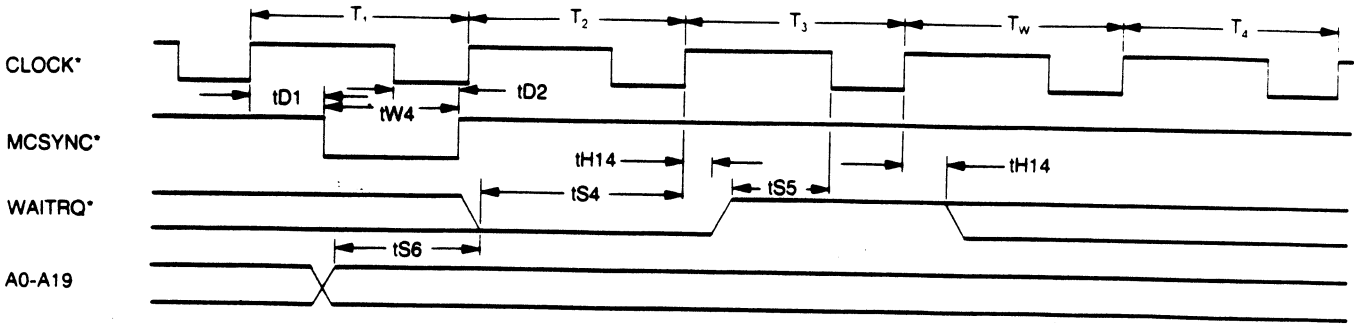


SYMBOL	PARAMETER	4.9152 MHz MIN	4.9152 MHz MAX
tD9	Delay from CLOCK* to Address 16-19		125
tD18	Delay from CLOCK* to INTAK* low	116	155
tD19	Delay from CLOCK* to INTAK* high	48	87
tD20	Delay from CLOCK* to Data Bus 3-State		51
tH13	Interrupt vector hold from CLOCK*	6	
tS3	Interrupt vector setup to CLOCK*	52	

All times given in nanoseconds

NOTE: The illustrated example does not show possible additional clock cycles between T4 of first cycle and T1 of second 'INTA' cycle. These clock cycles occur if the 8088's internal queue is not full. These clock cycles do not affect system operation, only total interrupt response time.

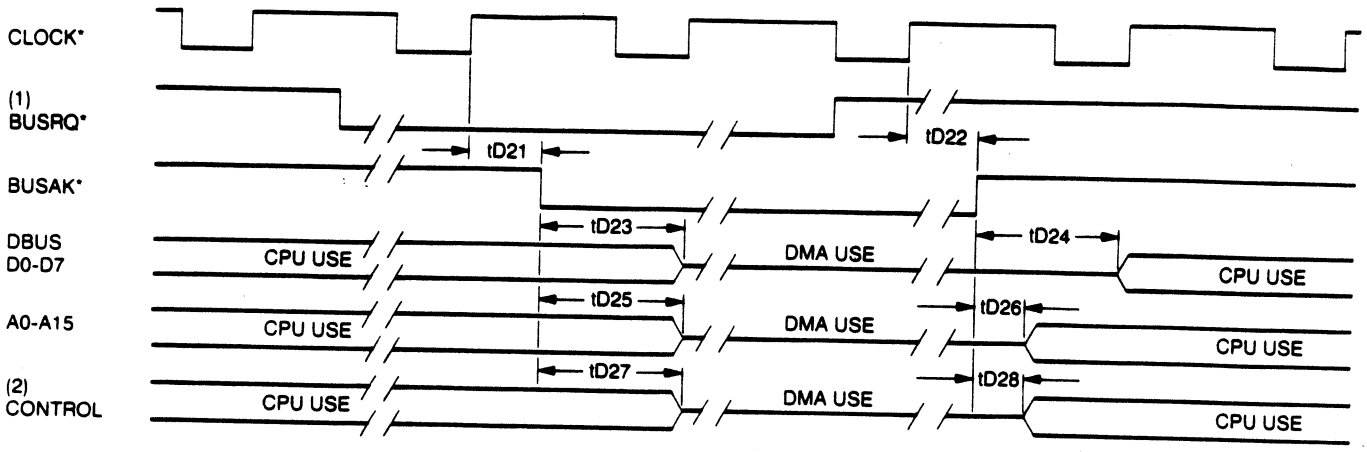
Figure 1-11. Bus Interrupt Timing



SYMBOL	PARAMETER	4.9152 MHz MIN	4.9152 MHz MAX
tD1	Delay from CLOCK* to MCSYNC* low	121	
tD2	Delay from CLOCK* to MCSYNC* high		102
tH14	WAITRQ* hold after CLOCK*	9	
tS4	WAITRQ* low setup to CLOCK*	26	
tS5	WAITRQ* high setup to CLOCK*	26	
tS6	Address 0-19 setup to WAITRQ*	256	
tW4	MCSYNC* pulse width	68	

All times given in nanoseconds

Figure 1-12. Bus Wait Request Timing



SYMBOL	PARAMETER	4.9152 MHz MIN	4.9152 MHz MAX
tD21	Delay from CLOCK* to BUSAK* low	0	178
tD22	Delay from CLOCK* to BUSAK* high	0	178
tD23	Delay from BUSAK* to Data Bus 3-state	-63	
tD24	Delay from BUSAK* to Data Bus driven	288	
tD25	Delay from BUSAK* to Address Bus 3-state	-88	
tD26	Delay from BUSAK* to Address Bus driven	212	
tD27	Delay from BUSAK* to Control Bus 3-state	-49	
tD28	Delay from BUSAK* to Control Bus driven	283	

All times given in nanoseconds

(1) Timings shown are for an asynchronous BUSRQ*.
(2) Control includes STD BUS lines MCSYNC*, IORQ*, MEMRQ*, RD*, WR*, STATUS0*, STATUS1*.

Figure 1-13. Bus Exchange Timing

SECTION 2. INSTALLATION

NOTE

This portion applies to the **7864-1** Multimaster Card; See Part II of this Addendum for **7864-3** Single Master Installation.

Pages 2-4 through 2-6, "CARD LAYOUT AND JUMPERS"

REPLACE with the following:

"The 7864-1 has onboard jumpers to configure the card to meet system requirements. The jumper configurations consist of wire jumpers and sockets as shown in Figure 2-3. The wire jumpers can be removed and installed without the use of soldering equipment. Figure 2-4 lists sources for the shorting connectors.

Figure 2-5 on the following pages provides a reference for the location and a brief description of each jumper on the 7864-1. The discussion following Figure 2-5 divides the jumper options into six functional groups: Multimaster Configuration, Reset, Memory and I/O, Interrupt, RS-422-A Serial Port, and RS-232-C Serial Port.

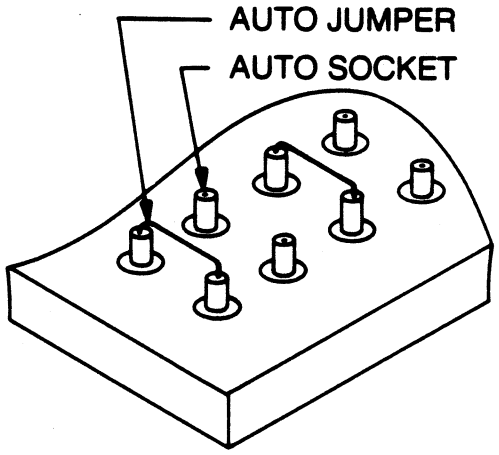


Figure 2-3. Jumper Configuration

SOURCE	PART NUMBER
Fancort Industries, Inc.	J 0.100X0.250 B 24
Squires Electronics, Inc.	J 0.100X0.250 B 24

Figure 2-4. Sources for Shorting Jumpers

U26 PAL Assembly Program Installation:

PAL Assembly Program #111829-XXX is installed in socket U26 for the 7864-1 for Multimaster operation. See Part II for the 7864-3 Single Master.

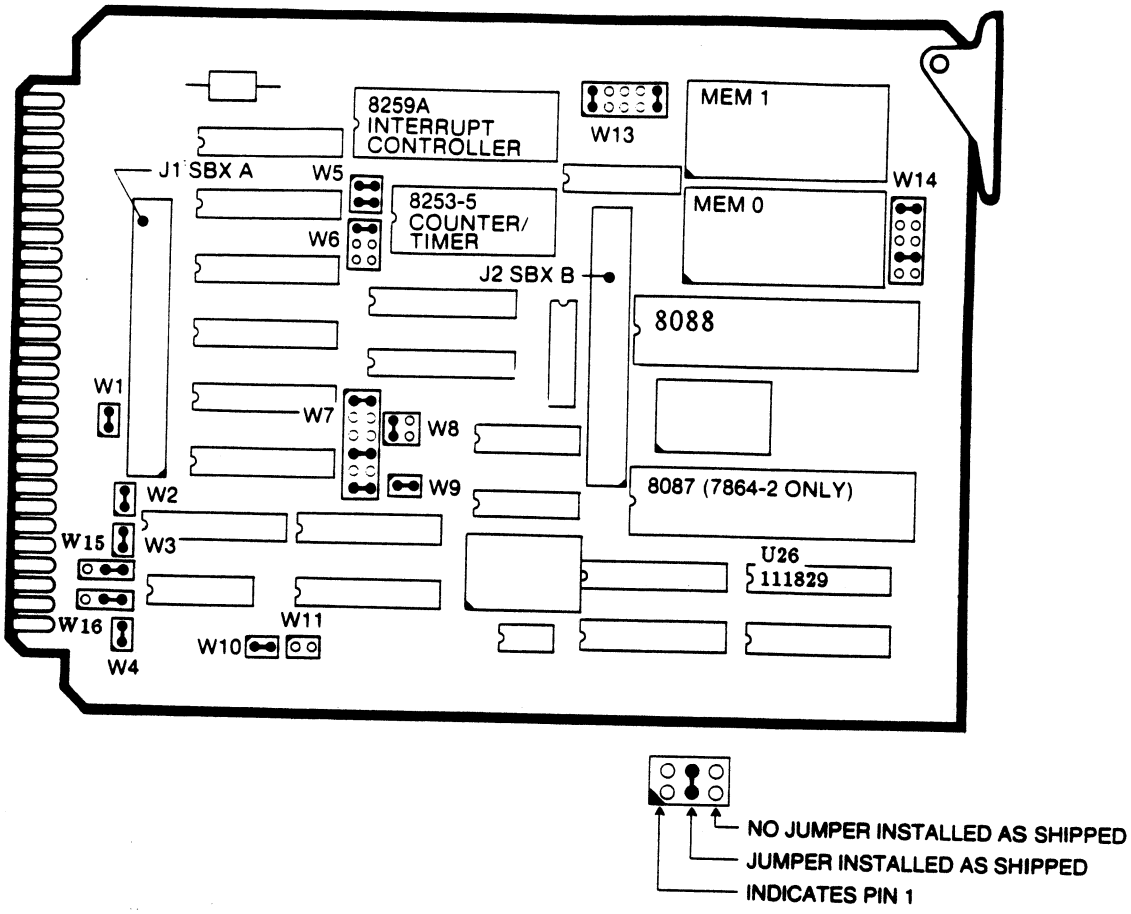


Figure 2-5. Physical Layout and Jumper Options

CHANGE: The following in the Jumper Options Table, Figure 2-5.

JUMPER GROUP	JUMPER INSTALLED	JUMPER REMOVED	DESCRIPTION	AS SHIPPED	SEE PAGE
W7	1-2 7-8,11-12	3-4,5-6 9-10	00000-01FFF FC000-FFFFF	* *	2-9 2-9
W13&W14	2-4,7-8,9-10	1-3,5-6	32K RAM		2-8

ADD:

W15&W16	2-3	1-2	PRO-LOG USE ONLY

CHANGE: Figure 2-13. Onboard Memory Mapping, Jumper W11. (As-shipped configuration change.)

MEM 0	OPTION 3	Pins 1-2 shorted
MEM 1	OPTION 1	Pins 7-8 and 11-12 shorted

SECTION 5. MAINTENANCE

NOTE

This information applies to both the 7864-1 and the 7864-3.

Pages 5-1 through 5-5, Schematic and Assembly Drawing

REPLACE with the new Schematic and Assembly Drawing attached.

NOTES: UNLESS OTHERWISE SPECIFIED

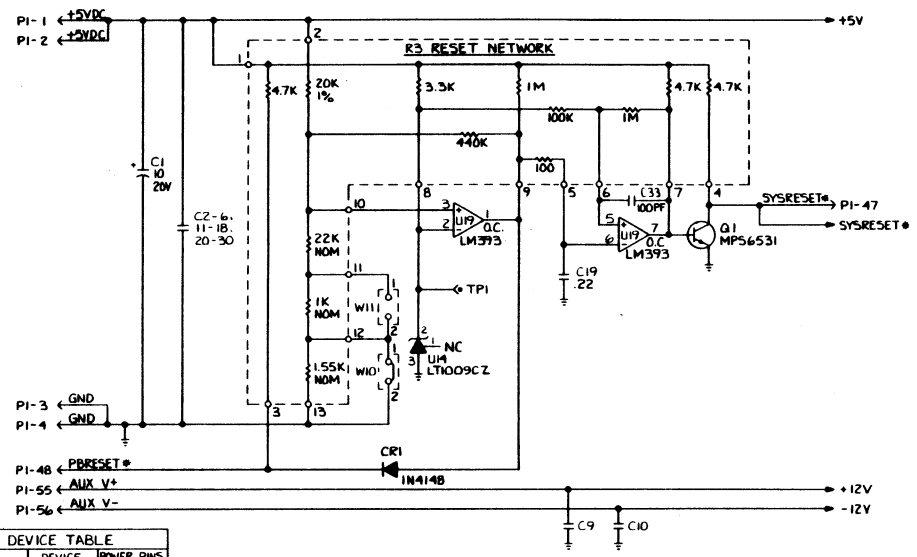
1. ALL CAPACITANCE VALUES ARE IN MICROFARADS, .1, 50V.
2. ALL RESISTANCE VALUES ARE IN OHMS, .25W, 5%.
   ALL RESISTOR NETWORK VALUES ARE IN OHMS, 1K, .1W, 2%.
3. CLOCK FREQUENCY AS SHIPPED IS 4.9152 MHZ.

4. FOR JUMPER CONFIGURATION, SEE TABLE.

5. PAL PROGRAM FOR U26:
   7864-1, MULTIMASTER IS PROGRAM NO. 111829.
   7864-2, MULTIMASTER IS PROGRAM NO. 111824.
   7864-3, SINGLE MASTER IS PROGRAM NO. 112357.

REVISIONS			
DOC REV	DESCRIPTION	DATE	APPR
A	INITIAL RELEASE PER PCN 3962	[illegible]	
B	REVISED PER PCN 4026	[illegible]	

REFERENCE DESIGNATION	
LAST USED	NOT USED
C33	C7, 31, 32
CR	
J2	
P1	
Q1	
R19	
TP1	
U27	
W16	W12
Y2	



SIGNAL LOCATOR CHART		
SIGNAL NAME	SHEET/ZONE LOCATION	
	SOURCE	DESTINATION
59INT	S3/C3	S3/B8
87INT	S2/C6	S3/D3
ADEN*	S2/B5	S2/D2
ALE	S2/B5	S3/B8
BUSINT	S2/C8	S3/D3, S3/B8
CAI3-CAI5	S2/D2	S3/C8
CAD0-CAD7	S2/D2	S3/D8
CNTLEN	S2/A5	S2/D3
CNTRL*	S2/B1	S2/B8
DEN*	S2/A6	S3/C8
DT/R*	S2/B5	S2/C2, S3/D8
HOSTLOCK*	S3/C5	S2/B8
INTAK	S3/B7	S2/B2
LA0-LA5	S2/D2	S3/A8
LOCK*	S3/C5	S2/B8
LS2*	S2/A2	S2/B8
MEM0*	S2/D3	S2/A7
MEMI*	S2/C3	S2/A7
PCI	S2/D2	S2/B8
PCO EN	S2/B5	S2/D2
PINTA	S2/B5	S3/B8
PINTR	S3/B7	S2/C8
PLOCK*	S2/C6	S3/B8
PRD*	S2/A6	S3/A8
PWR*	S2/A6	S3/A8
RESET	S2/C6	S3/A8
RESET*	S3/B6	S2/B8
RESINTA*	S3/B7	S2/A7
RESIO*	S3/C6	S2/A7
S0*-S2*	S2/C5	S3/B8
SBXWAIT*	S3/C2	S2/B8
SYSRESET*	S1/C3	S2/C8
CNTRL	S2/B2	S3/C7

DEVICE TABLE			
REF DES	DEVICE TYPE	POWER PINS	
		GND	+5V
U17	74ALS04	7	14
U13,26,27	PAL16R4A	10	20
U6,12	PAL16L8A	10	20
U24,25	PAL16R8A	10	20
U16	74AS08	7	14
U18	74ALS20	7	14
U9	8253-5	12	24
U8	8259A	14	28
U23	8087	1,20	40
U22	8088	1,20	40
U15	74ALS138	8	16
U7	74ALS240	10	20
U3-5	74ALS244	10	20
U1,10	74ALS245	10	20
U14	LT1009CZ	3	—
U2,11	74AS373	10	20
U19	LM393	4	8
U20	PROM	14	28
U21	RAM	14	28
R4-8,9	R-PACK	—	1
R2	R-PACK	—	14

4

DESCRIPTION	JUMPER POSITION									
	REF DES	PINS	REF DES	PINS	REF DES	PINS	REF DES	PINS	REF DES	PINS
7864-1 WITHOUT 8087	W3	1-2	W4	1-2	W8	1-2	W15	2-3	W16	2-3
7864-2 WITH 8087	W3	1-2	W4	1-2	W8	1-2	W15	2-3	W16	2-3
7864-3 WITHOUT 8087	W3	—	W4	—	W8	—	W15	1-2	W16	1-2

ITEM NO	QTY	DESCRIPTION
PARTS LIST		

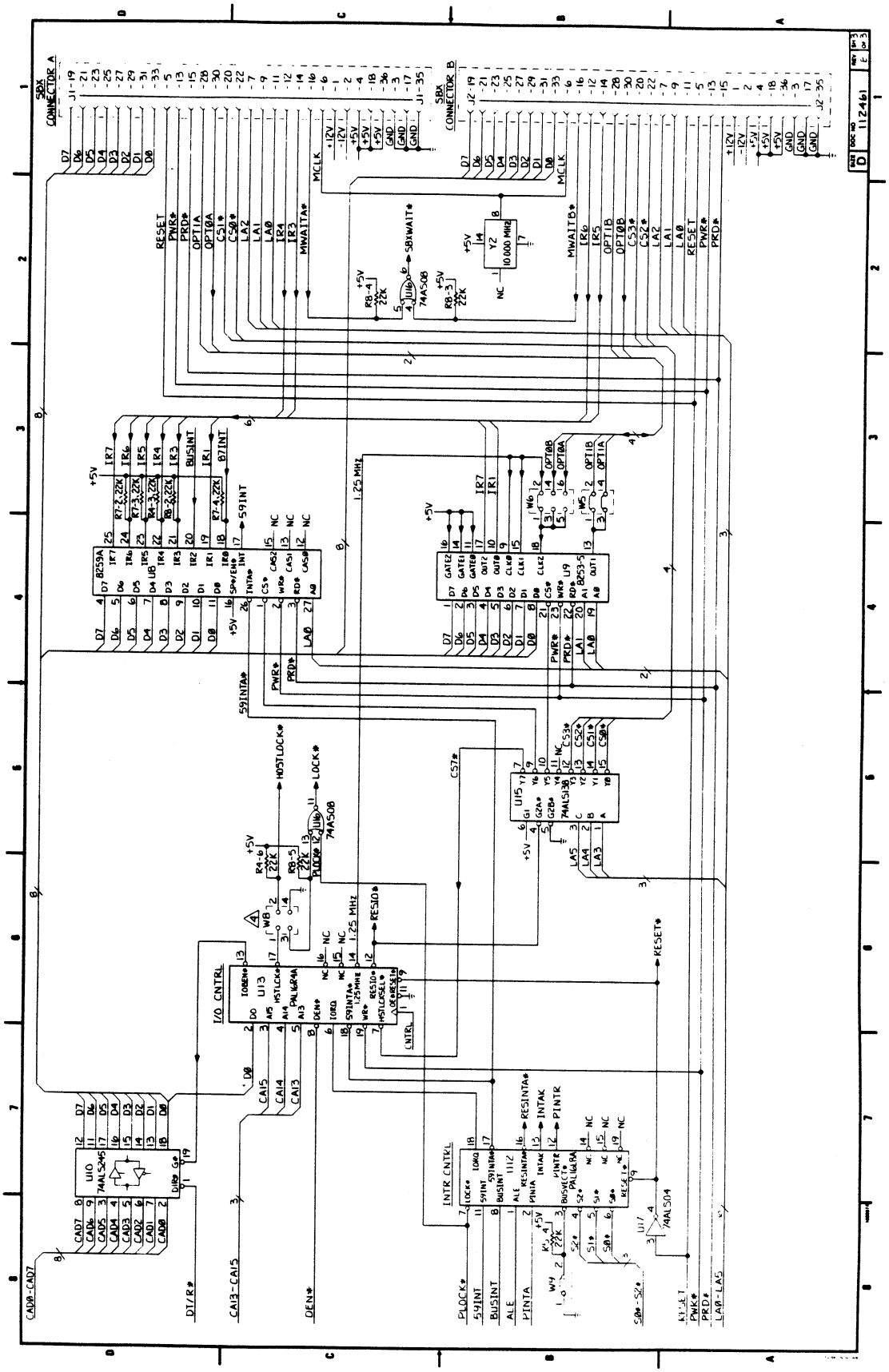
UNLESS OTHERWISE SPECIFIED
1. DIMENSIONS ARE IN INCHES
2. BREAK ALL SHARP EDGES
3. DO NOT SCALE DRAWING
4. TOLERANCES
   ANGLES ± —
   XX ± —
   XXX ± —

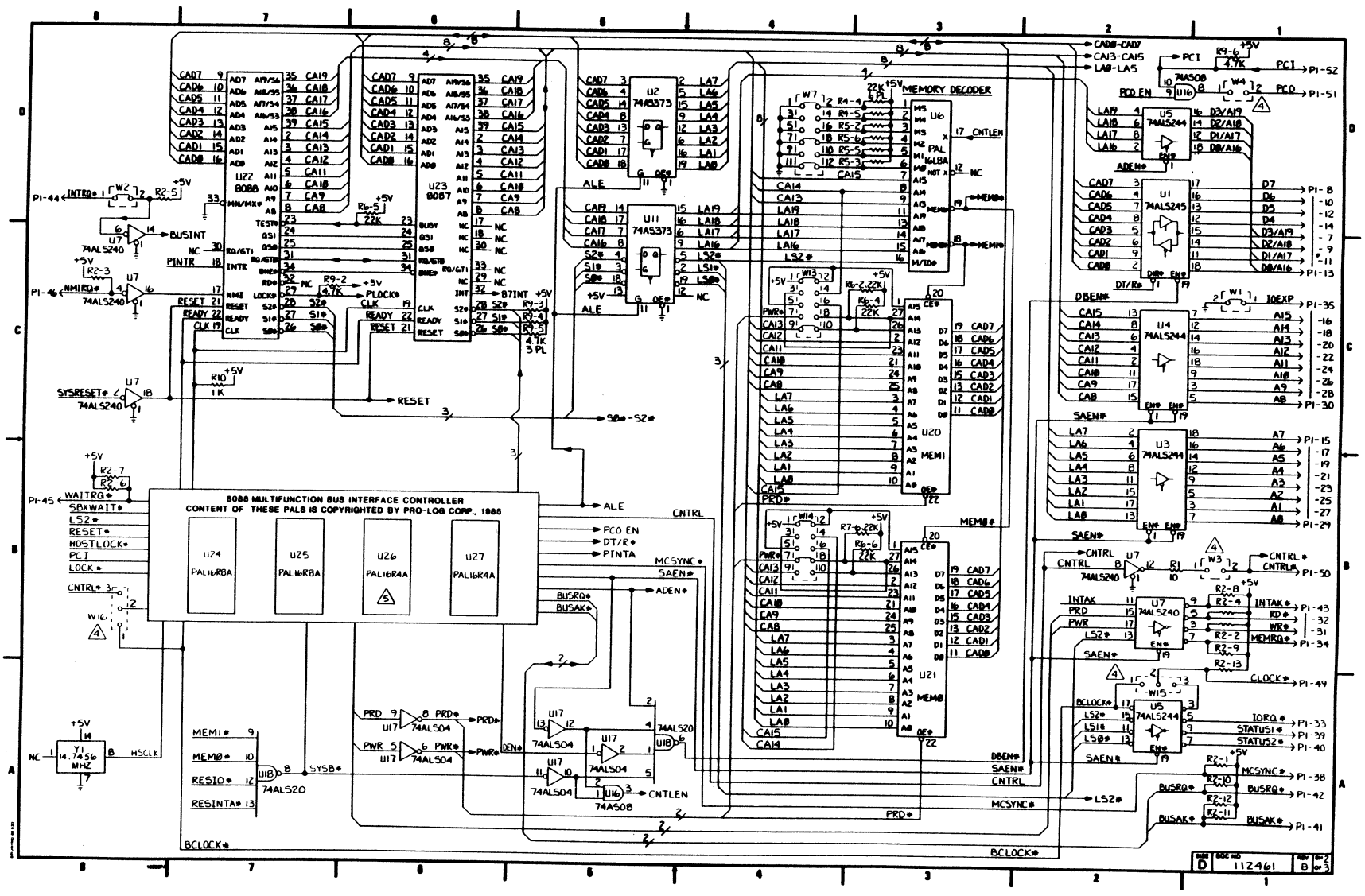
PRO-LOG CORPORATION

DRAWN P. LEE 11-7-84
CHECK E. GROSS 11-8-84
APPR [illegible] DATE [illegible]
SCALE NONE

TITLE: SCHEMATIC, 7864 8088 PROCESSOR CARD

SIZE D | DOC NO 112461 | REV C | SH 1 OF 3




8088 MULTIFUNCTION BUS INTERFACE CONTROLLER
CONTENT OF THESE PALS IS COPYRIGHTED BY PRO-LOG CORP., 1985
U24 PAL16R8A
U25 PAL16R8A
U26 PAL16R4A
U27 PAL16R4A
MEMORY DECODER
U22 8088
U23 8087
U2 74ALS373
U11 74ALS373
U6 PAL 16L8A
U20 MEM1
U21 MEM0
U1 74ALS245
U5 74ALS244
U4 74ALS244
U3 74ALS244
U7 74ALS240
U18 74ALS20
U17 74ALS04
U16 74ALS08
Y1 14.7456 MHZ
W1
W2
W3
W4
W5
W7
W8
W9
W10
W11
W12
W13
W14
W15
W16
INTRQ*
NMIRQ*
SYSRESET*
WAITRQ*
SBXWAIT*
LS2*
RESET*
HOSTLOCK*
PCI
LOCK*
CNTRL*
HSCLK
MEMI*
MEM0*
RESIO*
RESINTA*
SYSB*
BCLOCK*
BUSINT
PINTR
87INT
PLOCK*
ALE
PCO EN
DT/R*
PINTA
MCSYNC*
SAEN*
ADEN*
BUSRQ*
BUSAK*
CNTLEN
DBEN*
IOEXP
INTAK*
RD*
WR*
MEMRQ*
IORQ*
STATUS1*
STATUS2*
CLOCK*
CAD0-CAD7
CA13-CA15
LA0-LA5
PRD*
PWR*
D
112461
REV B
SHT 2 OF 3

NOTES: UNLESS OTHERWISE SPECIFIED.

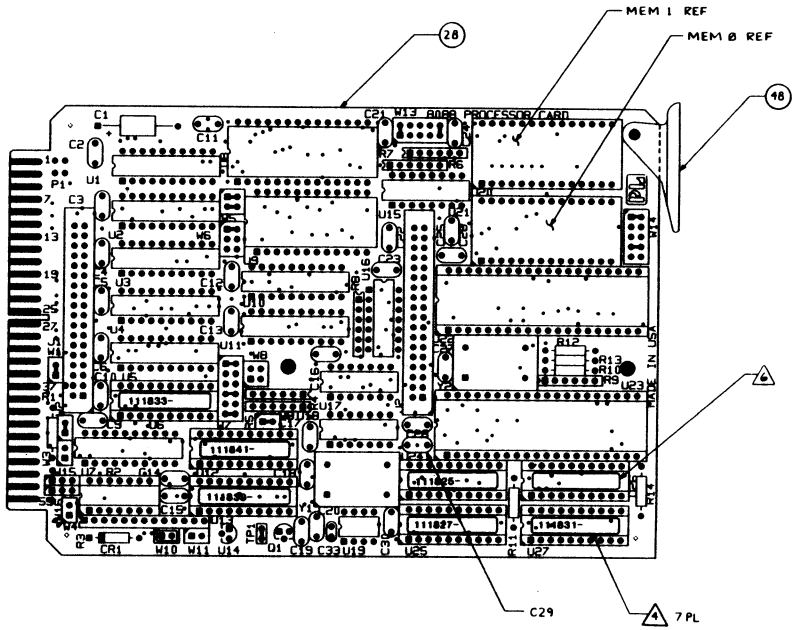
1. ASSEMBLY PART NUMBER IS 111703 -XXX .
2. THIS DOCUMENT AND PARTS LIST ARE TRACKING DOCUMENTS.
3. ASSEMBLY TO CONFORM TO WORKMANSHIP STANDARDS AS1004.

(4) PROGRAM U6, U12, U13, U24 THRU U27: MARK EACH LABEL WITH PROGRAM LISTING DASH NUMBER BEFORE ASSEMBLY.

(5) FOR JUMPER CONFIGURATION, SEE TABLE.

(6) REFERENCE PARTS LIST FOR CORRECT PAL ASSEMBLY INSTALLATION FOR U26.

REVISIONS			
DOC REV	DESCRIPTION	DATE	APPR
D	RE-DRAWN. FOR -004 THRU -006 SEE REV. C REVISED PER PCN 3782		



ASSEMBLY PART NO.	JUMPER POSITIONS									
	REF DES	PINS	REF DES	PINS	REF DES	PINS	REF DES	PINS	REF DES	PINS
111703-007	W3	1-2	W4	1-2	W8	1-2	W15	2-3	W16	2-3
111703-008	W3	1-2	W4	1-2	W8	1-2	W15	2-3	W16	2-3
111703-009	W3	—	W4	—	W8	—	W15	1-2	W16	1-2

SEE SEPARATE PARTS LIST

ITEM NO	QTY	DESCRIPTION
PARTS LIST		

UNLESS OTHERWISE SPECIFIED
1. DIMENSIONS ARE IN INCHES
2. BREAK ALL SHARP EDGES
3. DO NOT SCALE DRAWING
4. TOLERANCES:
ANGLES ± —
XX ± —
XXX ± —

PRO-LOG CORPORATION

DRAWN M. MARTINEZ 7-[illegible]-85
CHECK
APPR
DATE
SCALE 2:1

TITLE: ASSEMBLY, 8088 PROCESSOR CARD

SIZE D | DOC NO 111703 | REV D | SHT 1 OF 1

PART II

This segment of the Addendum covers the Installation, Operation, and Programming of the 7864-3 Multifunction Card. Please replace the appropriate sections in your manual with the attached pages.

The Counter/Timer and Interrupt Controller discussions have not changed, and therefore we are not including these discussions in this Addendum. Please see the Operation and Programming Section in the 7864 User's Manual.

Section 2
7864-3 INSTALLATION

INTRODUCTION

This section describes the procedures for installing the 7864-3 card in an STD BUS system and the jumper options that must be considered prior to installation.

POWER SUPPLY

CAUTION

To prevent possible damage to your STD BUS system, make sure power is off before inserting a card into the card rack or before removing a card from the card rack.

CAUTION

To guarantee proper operation of the 7864-3 card, LOGIC GND and AUX GND must be connected at the power supply.

Pro-Log power supplies are shipped with both GNDs tied together and therefore meet this requirement. If a source other than Pro-Log is used for power supplies, care must be taken to ensure this requirement is met.

In selecting a power supply for an STD BUS system that uses the 7864-3 card, make sure that all electrical requirements of the 7864-3 as specified in Section 1 (Electrical Specifications) are met. The 7864-3 can draw more than 2.5 amps of current from the 5V supply (Vcc) with memory installed. The power supply selected, the power distribution cables and connectors, and the STD BUS backplane must be able to supply the required current to each card while maintaining Vcc within the ±5% tolerance specified.

As shipped, the 7864-3 is held in a reset state until 60 milliseconds after Vcc reaches 4.75V minimum during power-up ensuring that the card is operated within specifications. Due to component tolerances in the reset circuitry, the actual level at which reset is released and operation begins may be as high as 4.90V. Voltage drops in cabling, connectors, and the STD BUS backplane may require that the power supply be adjusted before reset is released. See the following information on Reset, Jumper W5, for more information.

PHYSICAL INSTALLATION

The 7864-3 operates as part of an STD BUS system. A 7864-3 can be inserted into any slot in the STD BUS card rack, although some systems require certain physical arrangements of cards in the card rack. These arrangements are discussed in detail under "Priority Chain." When installed, the card ejector tab must be at the top as shown in Figure 2-1. If access to the card is needed for testing or servicing, a card extender such as the Pro-Log 7911 can be used. Card extenders tend to degrade STD BUS signals, which may cause problems with dynamic RAM or other STD cards with stringent bus timing or noise requirements. The use of more than one or two extenders may cause problems in any system.

The use of SBX modules on the 7864-3 increases the board height and occupies an additional 5/8-inch card slot.

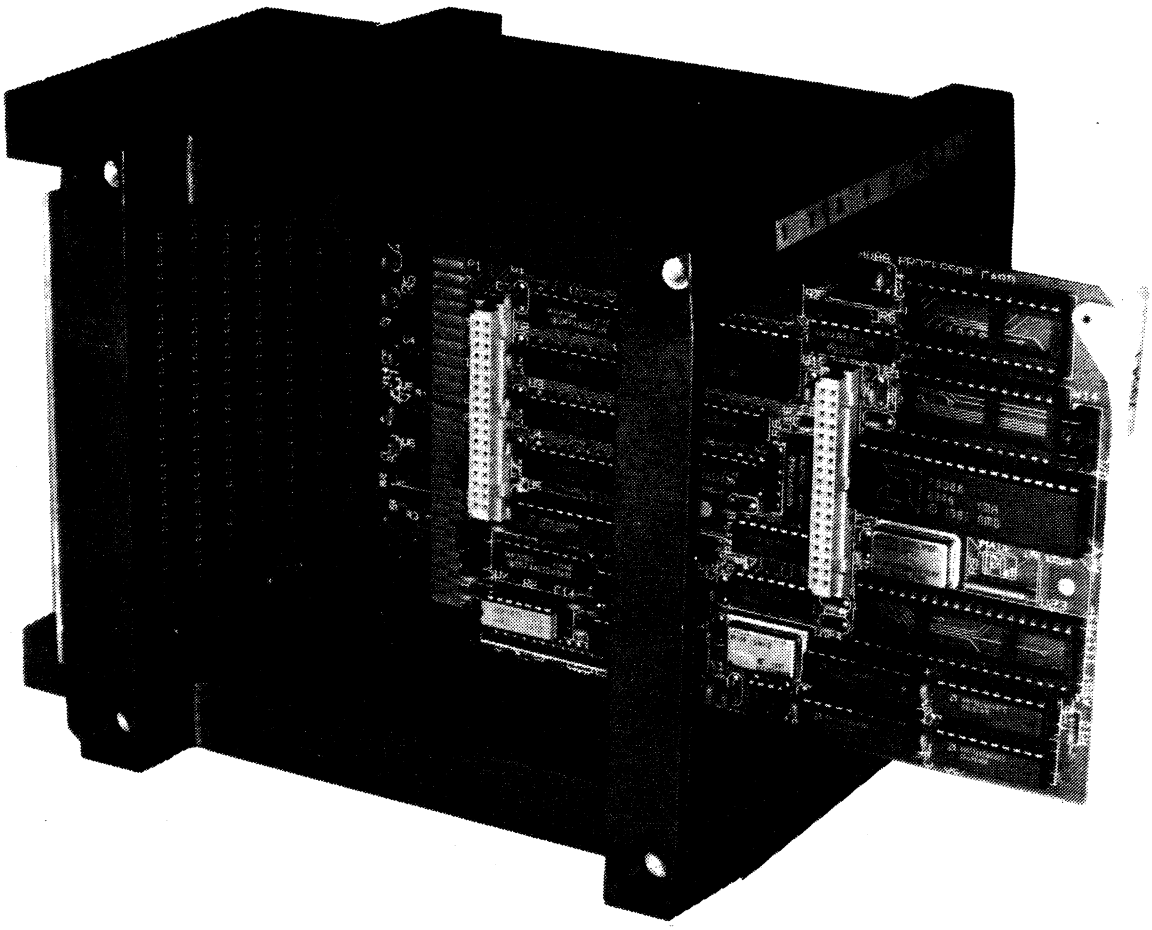


Figure 2-1. Installation

Priority Chain

The 7864-3 does not drive PCO, pin 51 on the STD BUS. Therefore, it is important to avoid placing the 7864-3 in a card slot within a group of STD cards utilizing the priority chain (such as I/O cards that use the chain for interrupt prioritization).

The priority chain lines on the STD BUS (PCO, pin 51, and PCI, pin 52) are used for serial interrupt or bus control. Two bus pins are allocated to the chain, which requires logic on-card to implement the serial priority function, or pass the priority chain through by connecting PCI to PCO onboard.

CARD LAYOUT AND JUMPERS

The 7864-3 has onboard jumpers to configure the card to meet system requirements. The jumper configurations are shown in Figure 2-2. The jumper wires can be removed and installed without the use of soldering equipment. Figure 2-3 lists sources for the shorting connectors.

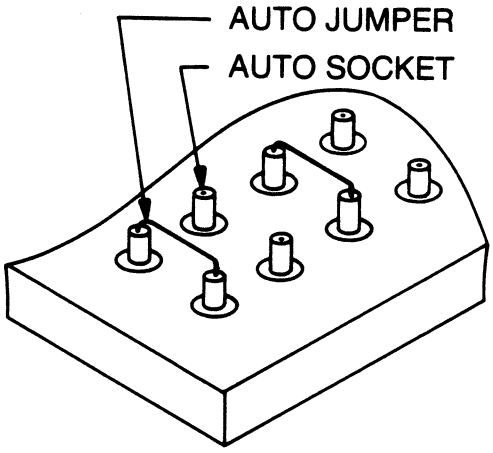


Figure 2-2. Jumper Configuration

SOURCE	PART NUMBER
Fancort Industries, Inc.	J 0.100X0.250 B 24
Squires Electronics, Inc.	J 0.100X0.250 B 24

Figure 2-3. Sources for Jumper Wires

Figure 2-4 provides a reference for the location and a brief description of each jumper on the 7864-3. The discussion following Figure 2-4 divides the jumper options into four functional groups: Reset, Memory and I/O, Interrupt, and SBX Connectors.

U26 PAL Assembly Installation

PAL Assembly 112337-XXX is installed in socket U26 for the 7864-3 Multifunction Card only.

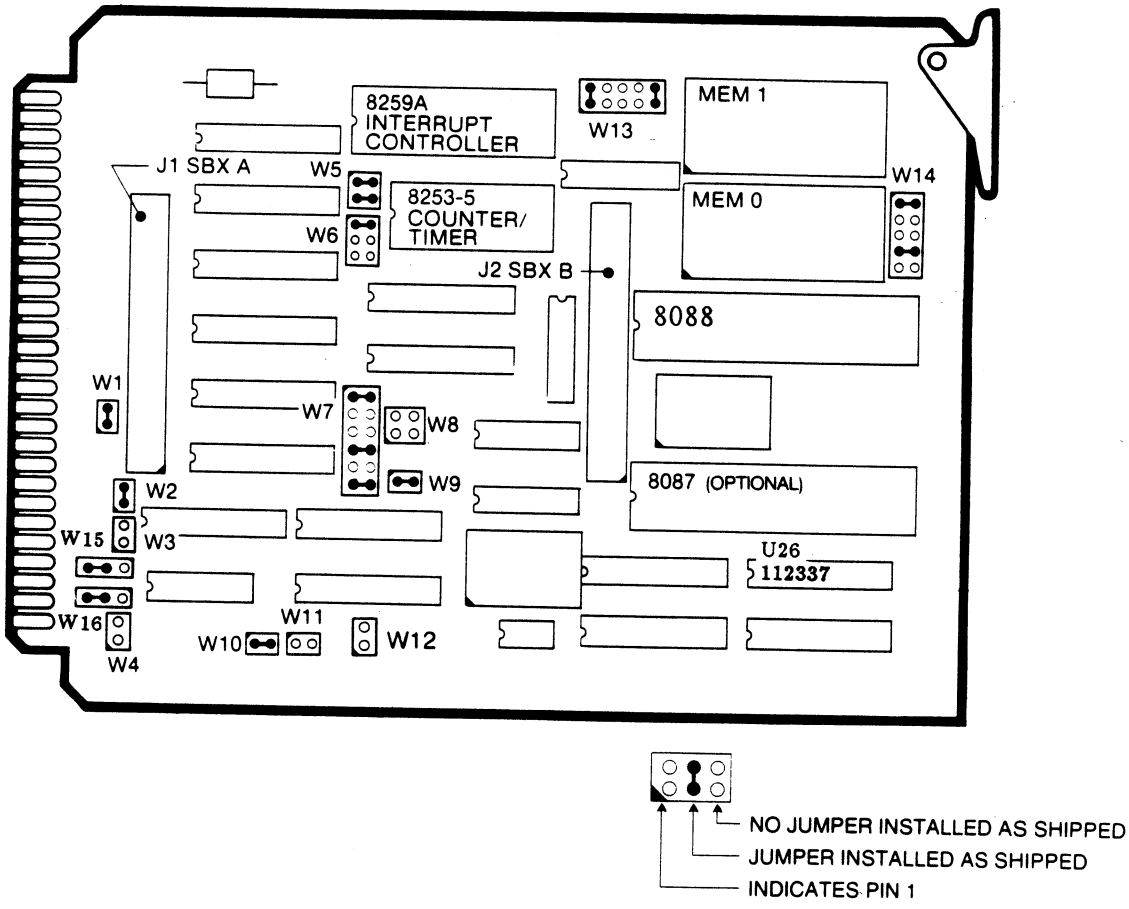


Figure 2-4. Physical Layout and Jumper Options

JUMPER GROUP	JUMPER INSTALLED	JUMPER REMOVED	DESCRIPTION	AS SHIPPED	SEE PAGE
W1	1-2 -	- 1-2	IOEXP DRIVE ENABLE * IOEXP grounded * IOEXP driven by another card	*	2-9
W2	1-2 -	- 1-2	BUS INTRQ* ENABLE * Enable * Disable	*	2-9
W3	PRO-LOG USE ONLY				
W4	PRO-LOG USE ONLY				
W5	3-4 1-2 1-2, 3-4	1-2 3-4 -	COUNTER/TIMER OPT1/OPT2 * OUT1 drives OPT1, SBX A * OUT1 drives OPT1, SBX B * OUT1 drives OPT1, both A&B	*	2-10
W6	5-6 3-4 1-2	3-4,1-2 5-6,1-2 3-4,5-6	OPTO/COUNTER/TIMER CLK 2 SOURCE * CLK2 input is OPTO, SBX A * CLK2 input is OPTO, SBX B * CLK2 input is 1.2288 MHz	*	2-10
W7	1-2,3-4,5-6 1-2,3-4 1-2,5-6 1-2 3-4,5-6 3-4 5-6 - 7-8,9-10,11-12 7-8,9-10 7-8,11-12 7-8 9-10,11-12 9-10 11-12 -	- 5-6 3-4 3-4,5-6 1-2 1-2,5-6 1-2,3-4 1-2,3-4,5-6 - 11-12 9-10 9-10,11-12 7-8 7-8,11-12 7-8,9-10 7-8,9-10,11-12	MEMORY MAPPING MEM0: (W7, Pins 1-2,3-4,5-6) * 00000-0FFFF (64K) * 00000-07FFF (32K) * 00000-03FFF (16K) * 00000-01FFF (8K) * E0000-EFFFF (64K) * F0000-F7FFF (32K) * FC000-FDFFF (8K) * SOCKET DISABLED MEM1: (W7, Pins 7-8,9-10,11-12) * F0000-FFFFF (64K) * F8000-FFFFF (32K) * FC000-FFFFF (16K) * FE000-FFFFF (8K) * 10000-1FFFF (64K) * 08000-0FFFF (32K) * 02000-03FFF (8K) * SOCKET DISABLED	* *	2-8
W8	1-2 1-3 2-4 -	3-4 2-4 1-3 1-2,3-4	LOCK MODE SELECT * DMA lock enable * Hardware lock enable * Lock always asserted (single CPU system) * Software lock only	*	2-7
W9	1-2 -	- 1-2	INTRQ* VECTOR SOURCE SELECT * Bus vector during INTAK* * SCC provides vector during INTAK*	*	2-10
W10	PRO-LOG USE ONLY				
W11	PRO-LOG USE ONLY				
W13	3-4,5-6,7-8 1-2,9-10 1-2,3-4,9-10 3-4,5-6,9-10 1-2,7-8 2-4,7-8,9-10	1-2,9-10 3-4,5-6,7-8 5-6,7-8 1-2,7-8 3-4,5-6,9-10 1-3,5-6	MEM1 CONFIGURATION * 8K ROM * 16K ROM * 32K ROM * 64K ROM * 8K RAM * 32K RAM	*	2-8
W14	3-4,5-6,7-8 1-2,9-10 1-2,3-4,9-10 3-4,5-6,9-10 1-2,7-8 2-4,7-8,9-10	1-2,9-10 3-4,5-6,7-8 5-6,7-8 1-2,7-8 3-4,5-6,9-10 1-3,5-6	MEM0 CONFIGURATION * 8K ROM * 16K ROM * 32K ROM * 64K ROM * 8K RAM * 32K RAM	*	2-8
W15 & 16	1-2	3-4	PRO-LOG USE ONLY		

Figure 2-4. (Continued)

Reset, Jumper W10 (Figure 2-5)

This jumper sets the voltage level to which Vcc on-card must rise before reset (and SYSRESET* on the STD BUS) is released, after time delay. As shipped, with a shorting connector installed in Jumper W10 pins 1-2, Vcc must reach +4.75V minimum. This ensures that all devices on the 7864-3 are operating within specification (Vcc = 5V ±5%) when reset is released. Due to component tolerances, the actual voltage level at which reset is released may be as high as 4.90V. Because of voltage drops in cabling and in the STD BUS backplane and card edge connectors, Vcc on the card may never rise above 4.90V and the card will not come out of the reset state. Adjustment of the power supply or remote sensing of Vcc on the backplane may be required.

Removal of the shorting connector from Jumper W10 lowers the Vcc voltage level at which reset is released to 4.75V maximum, 4.60V minimum. Adjustment of the power supply may not then be necessary. Note that if this shorting connector is removed, reset may be released to 4.75V and the card may be operated out of specification. Pro-Log recommends that you leave the W10 shorting connector in place and adjust Vcc at the power supply if necessary to ensure correct operation.

DESCRIPTION	PINS WITH SHORTING CONNECTORS INSTALLED
Power-on reset level is 4.75V minimum	1.2**
Power-on reset level is 4.75V maximum	NONE

**As shipped

Figure 2-5. Reset Voltage Select, Jumper W10

Memory and I/O

The 7864-3 has two memory sockets: MEM 1 and MEM 0. Jumpers W13 and W14, respectively, determine what type and size of memory device can be installed in each socket and Jumper W7 determines where each device is mapped in the 8088 CPU one-megabyte address range.

The 7864-3 memory sockets can accept JEDEC standard byte-wide ROMs and RAMs with an access time of 300 nanoseconds or less. Refer to Figure 2-6 for a list of recommended memory devices.

The only jumper that affects I/O is W1, which selects whether or not IOEXP, pin 35 on the STD BUS, is grounded onboard the 7864-3.

MEMORY TYPE	MEMORY TYPE	MFG. PART NUMBER	ACCESS TIME (ns)
EPROM	8K	Intel 2764	300 max.
	16K	Intel 27128 AMD 27128	
	32K	Intel 27256 AMD 27256	
	64K	Intel 27512	
RAM	8K	Hitachi HM6264 LP-15 Toshiba TC5565 PL-15	200 max.
	32K	NEC D4 3256 C-15	

Figure 2-6. Recommended Memory Devices

MEMORY SOCKET CONFIGURATION, JUMPERS W13 AND W14 (Figure 2-7)

These jumpers select what type of device is to be installed in sockets MEM 1 and MEM 0. Each socket can be independently configured to accept 8K, 16K, 32K, or 64K ROMs or 8K and 32K RAMs. Jumper W13 configures socket MEM 1 and W14 configures socket MEM 0.

DESCRIPTION	PINS WITH SHORTING CONNECTORS INSTALLED
8K ROM	1-2
16K ROM	1-2, 9-10[1]
32K ROM	1-2, 3-4, 9-10
64K ROM	3-4, 5-6, 9-10
8K RAM	1-2, 7-8[2]
32K RAM	2-4, 7-8, 9-10

[1] As shipped, W13 (MEM 1)
[2] As shipped, W14 (MEM 0)

Figure 2-7. Memory Socket Configuration Jumpers W13 (MEM 1) and W14 (MEM 0)

MEMORY MAPPING, JUMPER W7 (Figure 2-8)

Jumper W7 determines the mapping of the memory devices installed in sockets MEM 1 and MEM 0. Shorting connectors installed in pins 1 through 6 determine the mapping of the device in MEM 0; those installed in pins 7 through 12 determine the mapping of the device in MEM 1. There are eight mapping options for each socket. If the socket is not to be used (no memory device is to be installed), the last option should be selected disabling the socket and removing it from the memory map.

To prevent the selection of two options that map both sockets into the same address range, certain combinations of options for the two sockets cannot be used. For example, if MEM 0 Option 5 is selected, then MEM 1 Options 0, 2, 4, and 6 cannot be used. (MEM 0 Option 5 requires that no shorting connector be installed in W7 pins 11-12, while MEM 1 Options 0, 2, 4, and 6 require the installation of this jumper.) Unusable combinations occur only when Option 5 or 6 is selected for either socket; these options require that certain shorting connectors not be installed.

DESCRIPTION			PINS WITH SHORTING CONNECTORS INSTALLED	
SOCKET	OPTION	ADDRESS RANGE	PINS 1-6	PINS 7-12
MEM0:	0	00000-0FFFF (64K BLOCK)	1-2,3-4,5-6	
	1	00000-07FFF (32K BLOCK)	1-2,3-4	
	2	00000-03FFF (16K BLOCK)	1-2,5-6	
	3	00000-01FFF (8K BLOCK)**	1-2	DON'T CARE
	4	E0000-EFFFF (64K BLOCK)	3-4,5-6	
	5	F0000-F7FFF (32K BLOCK)	3-4	(No connector in 11-12)
	6	FC000-FDFFF (8K BLOCK)	5-6	(No connector in 9-10,11-12)
	7	SOCKET DISABLED	NONE	DON'T CARE
MEM1:	0	F0000-FFFFF (64K BLOCK)		7-8,9-10,11-12
	1	F8000-FFFFF (32K BLOCK)		7-8,9-10
	2	FC000-FFFFF (16K BLOCK)**	DON'T	7-8,11-12
	3	FE000-FFFFF (8K BLOCK)	CARE	7-8
	4	10000-1FFFF (64K BLOCK)		9-10,11-12
	5	08000-0FFFF (32K BLOCK)	(No connector in 5-6)	9-10
	6	02000-03FFF (8K BLOCK)	(No connector in 3-4,5-6)	
	7	SOCKET DISABLED	DON'T CARE	NONE

**As shipped

Figure 2-8. Onboard Memory Mapping, Jumper W7

For the most efficient use of memory space, the selected mapping option should use a block of memory of the same size as the device to be installed in the socket. For example, Option 2 for socket MEM 0 maps the socket at the address block 00000-03FFF hex, a 16-K block of memory; a 16K memory device should be used. If an 8K device is installed, it will be redundantly addressed in the upper half of the 16K block. If a 32K device is installed, the upper 16K of the device cannot be accessed. Additionally, two options should never be selected that map both sockets into the same address block.

IOEXP DRIVE, JUMPER W1 (Figure 2-9)

If a shorting connector is installed in Jumper W1 pins 1-2, IOEXP (pin 35 on the STD BUS) is connected to ground. If the connector is removed, IOEXP is not connected on the 7864-3 and can be driven by some other card in the system if necessary. IOEXP is defined in the 8088 Bus Specification as an enable line (low-level active) for I/O cards that decode an 8-bit I/O address instead of the 8088's full 16-bit address.

DESCRIPTION	PINS WITH SHORTING CONNECTORS INSTALLED
IOEXP grounded	1-2**
IOEXP driven by another card	NONE

**As shipped

Figure 2-9. IOEXP Drive Example Jumper W1

Interrupt Options

Jumpers W2 and W9 determine the response of the 7864-3 to maskable interrupt requests from the STD BUS (INTRQ*, pin 44).

INTRQ ENABLE, JUMPER W2 (Figure 2-10)*

If a shorting connector is installed in Jumper W2 pins 1-2, the 7864-3 can respond to INTRQ* on the STD BUS. If the connector is removed, the 7864-3 does not respond to INTRQ*.

DESCRIPTION	PINS WITH SHORTING CONNECTORS INSTALLED
This card responds to STD BUS INTRQ*	1-2**
Does not respond to STD BUS INTRQ*	NONE

**As shipped

Figure 2-10. INTRQ* Enable, Jumper W2

INTRQ VECTOR SOURCE SELECT, JUMPER W9 (Figure 2-11)*

The 8088 CPU responds to a maskable interrupt request by executing an interrupt acknowledge cycle during which an 8-bit vector is read in on the processor data bus. This vector is normally provided by the interrupting device and is used by the processor to locate the correct interrupt service routine. If a shorting connector is installed in Jumper W9 pins 1-2, the 8088 executes an interrupt acknowledge cycle and reads a vector (which must be supplied by the interrupting device) from the STD data bus in response to an STD BUS INTRQ*.

When the shorting connector is removed from Jumper W9, INTRQ* can no longer directly cause an 8088 maskable interrupt. However, INTRQ* is permanently connected (through a buffer) to one of the interrupt request inputs (IR1) of the 8259A Interrupt Controller. The Interrupt Controller can generate an onboard interrupt in response to INTRQ* and provide a vector on-card when the interrupt is acknowledged.

DESCRIPTION	PINS WITH SHORTING CONNECTORS INSTALLED
Vector read from STD BUS during INTAK*	1-2**
Interrupt Controller provides vector during INTAK*	NONE

**As shipped

Figure 2-11. INTRQ* Vector Source Select, Jumper W9

SBX Connector Option Lines

These jumpers allow one input and one output from the counter/timer to be brought out to the SBX connectors on the SBX option lines (OPT0 and OPT1).

OPT1/COUNTER/TIMER CHANNEL 1 OUTPUT, JUMPER W5 (Figure 2-12)

The output from channel 1 of the counter/timer can be brought out to the SBX connectors using this jumper, providing a programmable clock for SBX modules. Insertion of a shorting connector in pins 1-2 connects the output to option line 1 of SBX connector B; a shorting connector in pins 3-4 connects the output of option line 1 of SBX connector A.

Pins 2 and 4 of this jumper group also serve as the required wirewrap posts on the SBX baseboard (the 7864-3) which are connected to option line OPT1 on SBX connectors A and B respectively. If a user-supplied SBX module requires some other signal from the 7864-3, it can be wirewrapped to these pins.

DESCRIPTION	PINS WITH SHORTING CONNECTORS INSTALLED
Counter/Timer OUT1 drives OPT1, SBX A	3-4
Counter/Timer OUT1 drives OPT1, SBX B	1-2
Counter/Timer OUT1 drives OPT1A & OPT1B	1-2, 3-4**

**As shipped

Figure 2-12, OPT1/Counter/Timer Chan. 1 Output, Jumper W5

OPT0/COUNTER/TIMER CLK2 INPUT, JUMPER W6 (Figure 2-13)

This jumper selects the source for the clock input of counter/timer channel 2. If a shorting connector is inserted in pins 3-4 or 5-6, the source of the channel 2 clock is option line 0 from either SBX connector A or B respectively. This allows channel 2 of the counter/timer to serve as a counter for some SBX function.

If a shorting connector is inserted in jumper W6, pins 1-2, the clock source is the same as that of the other counter/timer channels: a 1.2288 MHz signal generated onboard the 7864-3.

Pins 4 and 6 of this jumper group also serve as the required SBX baseboard wirewrap posts which are connected to option line OPT0 on SBX connectors A and B respectively. If a user-supplied SBX module requires some other signal from the 7864-3, it can be wirewrapped to these pins.

DESCRIPTION	PINS WITH SHORTING CONNECTORS INSTALLED
Counter/Timer CLK2 source is OPT0, SBX A	5-6
Counter/Timer CLK2 source is OPT0, SBX B	3-4
Counter/Timer CLK2 source is 1.2288 MHz	1-2**

**As shipped

Figure 2-13. Counter/Timer Chan. 2 Clock Source Select, Jumper W8

7864-3 OPERATION AND PROGRAMMING

INTRODUCTION

This section includes a general discussion of the operation of the 7864-3 Multifunction CPU/SBX card and the programming required to initialize and use the 7864-3 onboard functions. These functions include the reset circuit, interrupts, and memory and I/O addressing.

SINGLE-CPU SYSTEMS

The 7864-3 is used as the sole CPU card in a system in the same way that STD BUS systems have always been implemented in the past -- with only one CPU card in the card rack. The 7864-3 always controls the STD BUS unless DMA operations are used.

OPERATION AND PROGRAMMING

Reset

The 7864-3 resets the 8088 CPU, the 8087 Math Coprocessor, and certain onboard logic upon entering a reset state. The STD BUS signal SYSRESET* is also driven active (low) during this time. The source of the reset can be either the onboard power-on/DC power-fail circuitry or pushbutton or system reset from the STD BUS.

POWER-ON/DC POWER-FAIL RESET

The 7864-3 uses a precision voltage reference and comparator to monitor the level of Vcc on-card. During power-on, the reset state is held for 60 milliseconds after Vcc has reached 4.75V minimum. This ensures that all components on the card are operating within specification (Vcc = 5V ± 5%) when reset is released. Reset is also asserted when Vcc on-card falls below a specified level. Refer to Section 1, Electrical Specifications, for exact voltage levels and tolerances. Under certain conditions, adjustment of the power supply or a jumper change in the reset circuit may be required before reset will be released and the 7864-3 begins operation. See the jumper reset options in Section 2, Installation.

PUSHBUTTON RESET

The 7864-3 can be forced into a reset state with an active (low) level on the STD BUS pushbutton reset (PBRESET*) signal. PBRESET* can be either controlled by a switch or driven with an open collector device. The signal is debounced on-card and must remain low for a minimum of 5 milliseconds to guarantee a reset.

SYSTEM RESET

An active (low) level on the STD BUS system reset signal (SYSRESET*) will also cause a 7864-3 reset. (The 7864-3 will not drive SYSRESET* in response to this reset.) This signal is not debounced and should be driven only by circuitry specifically designed for this purpose (such as an AC power-fail detect card or the reset circuitry on another STD card).

When reset is released, program execution begins at physical address FFFF0 hex (code segment = FFFF hex, instruction pointer = 0000 hex).

Interrupts

Every 8088 interrupt has a type number that identifies it to the CPU. The type number is used in the 8088 vectored interrupt scheme. It is a single-byte value that the CPU internally multiplies by four to form a pointer. The pointer points to an interrupt table in segment 0000 hex containing the address of the interrupt service routine. The multiplication of the type number (vector) by four allows the complete physical address (Code Segment and Instruction Pointer, two 16-bit numbers) of the interrupt service routine to be stored in the interrupt table as four consecutive bytes.

The 7864-3 8088 CPU can respond to both internal and external (to the CPU) interrupts. Sources for external interrupts on the 7864-3 can include the STD BUS signals NMIRQ* (nonmaskable interrupt request) and the INTRQ* (interrupt request) and the onboard 8259A Interrupt Controller.

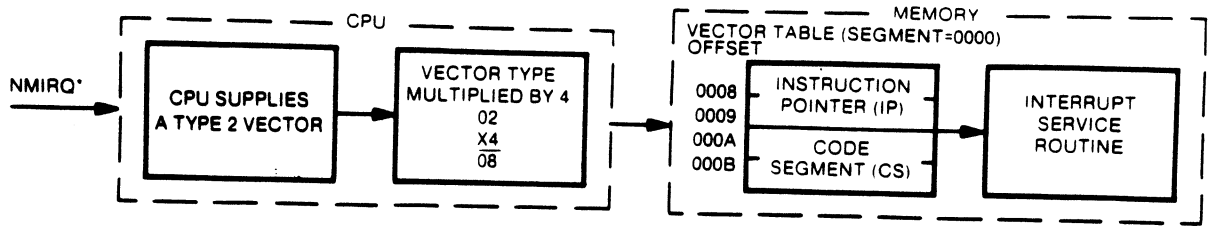


Figure 3-1. NMIRQ* Processing

Nonmaskable interrupt requests on the STD BUS NMIRQ* signal are predefined by the 8088 as Type 2 interrupts and no other vector is needed. Figure 3-1 shows how the CPU processes an NMIRQ*. A Type 2 interrupt has a higher priority than any other external interrupt and since it is nonmaskable (the CPU always responds to a Type 2 interrupt at the end of its current instruction cycle), NMIRQ* is generally used to signal the CPU of a "catastrophic" event

Interrupt requests on the STD BUS INTRQ* signal and from the onboard Interrupt Controller are not assigned a type number by the CPU. The interrupting device must provide the type number (or vector) on the CPU's data bus during the interrupt acknowledge cycle. Figure 3-2 shows how the 8088 processes these interrupts. The 7864-3 differentiates between STD BUS INTRQ* and interrupt requests from the onboard Interrupt Controller; INTRQ* has a higher priority than onboard interrupts. When the 7864-3 responds to an onboard interrupt request, it is assumed that the vector will be generated on-card (by the Interrupt Controller) and an STD BUS access is not attempted during the interrupt acknowledge cycle.

The 7864-3 responds to an STD BUS INTRQ* by gaining bus access, executing an interrupt acknowledge cycle, and reading the type number (vector) supplied by the interrupting device from the STD BUS data bus.

The 7864-3 is capable of generating a vector onboard. INTRQ* is connected (through a buffer) to one input of the Interrupt Controller. The controller can generate an interrupt when INTRQ* is active and provides the required on-card vector when the interrupt is acknowledged. This onboard vector capability allows the use of cards that can generate INTRQ* but not an 8088 vector in a 7864-3 system. The shorting connector should be removed from Jumper W9 if this onboard INTRQ* response is to be used, so that the 7864-3 does not respond to an STD BUS INTRQ* with a bus interrupt acknowledge cycle.

If the shorting connector is removed from Jumper W3 on the 7864-3, the card will not respond to STD BUS INTRQ* at all. Refer to Interrupt Options in Section 2 for more information on maskable interrupt response.

The 8087 Math Coprocessor can generate interrupts when certain internal conditions or "exceptions" (such as stack overflow or underflow or indeterminate operations such as divide by zero) are detected. The 8087 interrupt output drives one input of the Interrupt Controller, which provides an on-card interrupt and vector for 8087 interrupts. Other onboard interrupts can be generated through the Interrupt Controller by the counter/timer and by the user-supplied SBX I/O modules. See the section following on Interrupt Controller operation and programming.

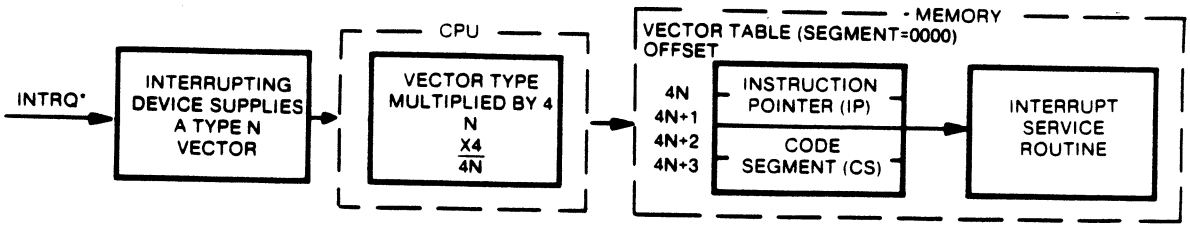
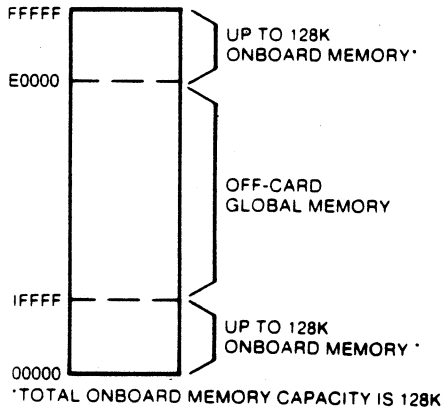


Figure 3-2. INTRQ* Processing

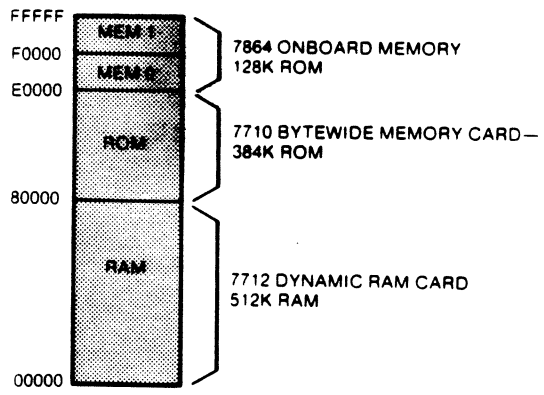
Memory Addressing

The 7864-3 8088 CPU provides a 20-bit memory address during each memory operation so the 7864-3 can direct address 2^{20} (1,048,576 or 1M) bytes of memory. The two onboard memory sockets can be configured to support various sizes of memory devices and can be mapped at different locations within the one megabyte memory map. See Figure 2-13 for onboard memory mapping options. Generally, one memory socket is mapped at the high end of memory to support the 8088 power-on restart address (FFFF0 hex) while the other is mapped at the low end to include the 8088 interrupt vector table (00000 to 007FF hex).

When the 7864-3 is addressing off-card memory, the lower 16 address bits are output on address lines A0-A15 on the STD BUS. The upper four bits (A16-A19) are time multiplexed onto the STD data bus (bits D0-D3) at the beginning of each machine cycle. Memory cards used in 8088 STD systems latch these upper address lines on the rising edge of STD BUS control signal MCSYNC*.



A



B

Figure 3-3. Memory Mapping Examples

MEMEX is defined in the 8088 STD BUS specification as an enable for memory cards that only decode a 16-bit memory address. No provision is made for driving MEMEX on the 7864-3 and only memory cards with the onboard latch required to decode the full 20-bit 8088 address should be used with the 7864-3 to avoid redundant addressing of memory.

Several examples of memory mapping in 7864-3 STD systems are shown in Figure 3-3.

I/O Addressing

The 7864-3 8088 CPU provides a 16-bit I/O port address during each I/O operation and can directly address 2^{16} (65,536 or 64K) I/O port locations. As with memory, onboard I/O (the Interrupt Controller, Counter/Timer and SBX modules) can be read from or written to without having access to the STD BUS.

Due to onboard decoding limitations, the upper 8K of the 64K I/O address field is reserved for onboard I/O even though only 38 port addresses are actually used. The lower 56K (Ports 0000-DFFF hex) is available for common or global I/O that can be addressed by all multimasters in the system. See Figure 1-5 for 7864-3 I/O mapping. Figure 3-4 shows the mapping of user-supplied SBX modules when installed in SBX connectors A and B. Note that Ports E000-FFBF, FFE0-FFE7, FFEC-FFEF, and FFF2-FFFE hex should never be accessed since the onboard I/O devices will be redundantly addressed in these address ranges.

SBX MODULE	SBX CHIP SELECT	I/O ADDRESS RANGE
A	MCS0* MCS1*	FFC0-FFC7 FFC8-FFCF
B	MCS0* MCS1*	FFD0-FFD7 FFD8-FFDF

Figure 3-4. SBX Module Mapping

Most existing STD BUS I/O cards decode only an 8- or 10-bit I/O address since few systems need more than 256 or 1024 ports. The full port address range of these cards (00-FF for 8-bit or 000-3FF for 10-bit) is available. Indirect (16-bit) addressing should be used when addressing 10-bit I/O cards to allow the card to distinguish between onboard and off-card ports; 8-bit I/O cards can be directly addressed in Page 0 of the I/O address space. Eight- and ten-bit I/O cards are not usually used together in the same system since port addresses would have to be selected with great care to avoid redundant addressing ("shadow" ports).

Provision is made for grounding the STD BUS IOEXP signal onboard the 7864-3 since many 8-bit address I/O cards use this signal as an enable input. Several examples of I/O port configurations in 7864-3 systems are shown in Figure 3-5.

NOTE

There are no changes to the Counter/Timer and Interrupt Controller portions of Section 3 of the 7864 User's Manual. Refer to the manual for information.

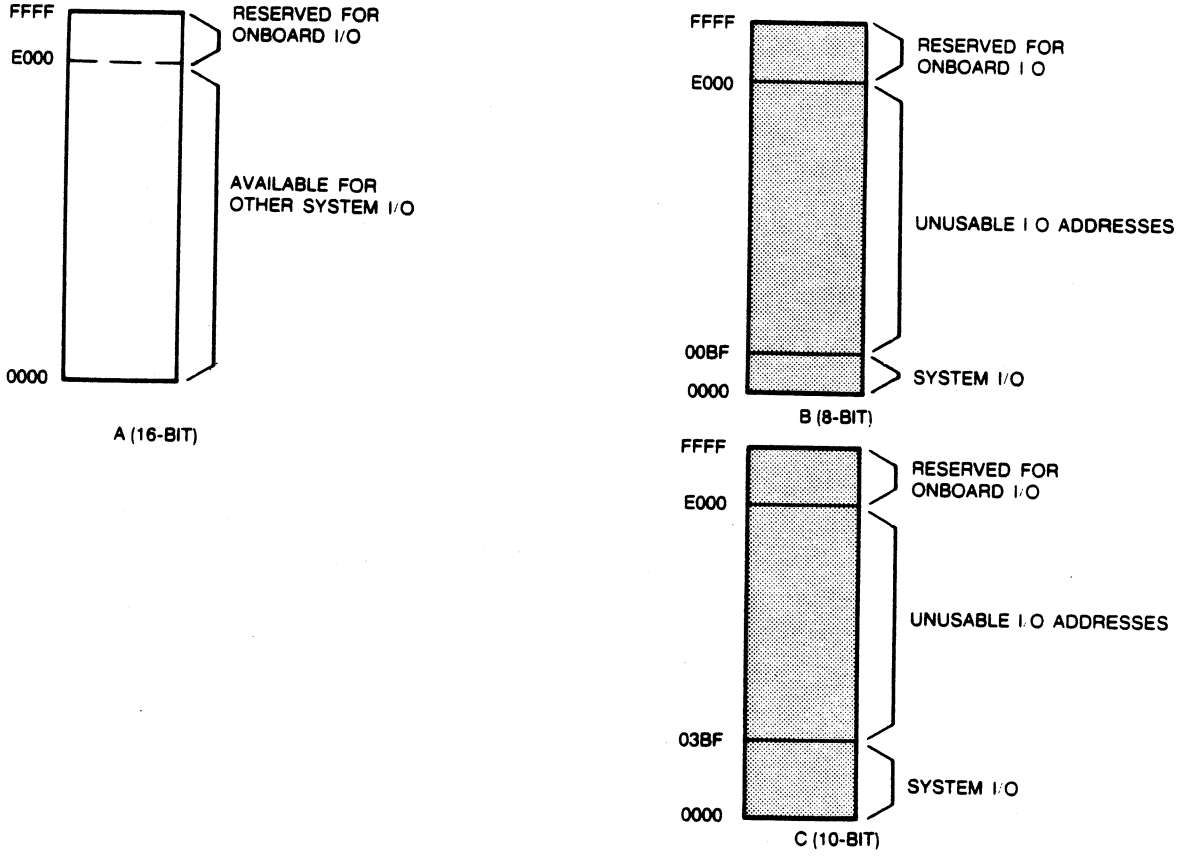


Figure 3-5. I/O Port Configuration Examples

Pro-Log reserves the right to make changes to any products herein to improve reliability, function or design. Pro-Log does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights nor the rights of others.

PRO-LOG® CORPORATION
2560 Garden Road, Monterey, California 93940
Phone: (408) 372-4593, (800) 538-9570
Telex: 171879, TWX: 910-360-7082